IMPROVED FLIP CHIP BALL GRID ARRAY PACKAGE

FIELD OF THE INVENTION

[0001] This is a continuation-in-part of United States patent application serial no. 10/211,567 entitled Improved Chip Scale Integrated Circuit Package, filed August 5, 2002.

FIELD OF THE INVENTION

[0002] The present invention relates in general to integrated circuit packaging, and more particularly to a flip chip ball grid array package with improved thermo-mechanical properties.

BACKGROUND OF THE INVENTION

[0003] High performance integrated circuit (IC) packages are well known in the art. Improvements in IC packages are driven by industry demands for increased thermal and electrical performance and decreased size and cost of manufacture

[0004] In general, array packaging such as Ball Grid Array (BGA) packages provide a high density of interconnects relative to the surface area of the package. Typical BGA packages include a convoluted signal path, giving rise to high impedance and an inefficient thermal path which results in poor thermal dissipation performance. With increasing package density, the spreading of heat generated by the device is increasingly important.

[0005] Direct connection of the semiconductor die to a substrate surface in a flip-chip orientation, using solder ball connections provides low impedance packages relative to the use of wire-bond connections and provides reduced package space. This technology is becoming increasingly popular with package fabrication advances including advances in forming and placing of solder balls in flip-chip packaging.

[0006] Figure 1 shows a sectional view of a conventional flip-chip BGA package indicated generally by the numeral 20. The flip-chip BGA package includes a substrate 22 with a semiconductor die 24 mounted in a flip-chip orientation, to a first surface of the substrate 22. Solder balls 26 provide electrical connections between the semiconductor die 24 and the substrate 22. Solder balls 28, in the form of a ball grid array are disposed on the second

surface of the substrate. These packages suffer disadvantages, however.

[0007] One particular disadvantage is the generation of thermally induced stress in these packages, due to a mismatch in coefficients of thermal expansion (CTE) between the semiconductor die and the motherboard, when the package is in use. During temperature cycling, the CTE mismatch creates stresses and strains which are concentrated in the solder ball interconnects between the die and the substrate and in the semiconductor die. In extreme cases, the semiconductor die warps and fatigue failure occurs in the solder ball interconnects.

[0008] Variations to the conventional flip-chip BGA have been proposed for the purpose of increased performance. In one exemplary variation, a metal heat spreader is fixed to the back of the semiconductor die to aid in the dissipation of heat. While heat is better dissipated in this package than in the conventional flip-chip BGA, described above, CTE mismatch between the semiconductor die and the motherboard, still cause stresses and strains that have deleterious effects on the package integrity.

[0009] Thus, further improvements in flip-chip ball grid array packages are desirable in order to meet industry demands for increased performance.

SUMMARY OF THE INVENTION

[0010] In one aspect of the present invention, a flip-chip ball grid array integrated circuit package with improved thermo-mechanical properties is provided. The package includes a substrate having first and second surfaces and a plurality of conductive traces therebetween. A semiconductor die is flip-chip mounted to the first surface of the substrate and electrically connected to ones of the conductive traces. An intermetallic heat spreader is fixed to a back side of the semiconductor die and a plurality of contact balls are disposed on the second surface of the substrate. The contact balls are in the form of a ball grid array and ones of the contact balls of the ball grid array are electrically connected with ones of the conductive traces.

[0011] In another aspect of the present invention, an integrated circuit package is provided. The integrated circuit package includes a substrate having first and second surfaces and a plurality of conductive traces therebetween. A semiconductor die is flip-chip mounted to the first surface of the substrate and electrically connected to ones of the conductive traces. A heat spreader having a coefficient of thermal expansion in the range of about 18 ppm/°C to about 26

ppm/°C, is fixed to a back side of the semiconductor die, and a plurality of contact balls are disposed on the second surface of the substrate, in the form of a ball grid array. Ones of the contact balls of the ball grid array are electrically connected with ones of the conductive traces.

[0012] Advantageously, the use of an intermetallic compound, such as copper aluminide, fixed directly to a silicon wafer provides an effective heat spreader for dissipating heat away from the semiconductor die of the IC package. In one aspect, the intermetallic compound has a coefficient of thermal expansion that is close to that of a typical motherboard and an elastic modulus that is high to restrain the semiconductor die thereby reducing stress at the solder ball interconnects and inhibiting the die from warping.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The present invention will be better understood with reference to the drawings and the following description, in which:

[0014] Figure 1 is a sectional view of a conventional flip-chip ball grid array package;

[0015] Figure 2 is a sectional view of flip-chip ball grid array package according to a first embodiment of the present invention;

[0016] Figure 3 is a sectional view of a flip-chip ball grid array package according to a second embodiment of the present invention; and

[0017] Figure 4 is a sectional view of a flip-chip ball grid array package according to a third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] Reference is now made to Figure 2 to describe a first embodiment of a flip chip ball grid array (BGA) package 20, indicated generally by the numeral 120. To simplify the description, the numerals used previously in describing Figure 1, will be used again after raising the numerals by 100 where parts to be described correspond to parts already described.

[0019] The flip-chip BGA package 120 includes a substrate 122 having first and second surfaces and a plurality of conductive traces therebetween. A semiconductor die 124 is flip-chip

mounted to the first surface of the substrate 122 and electrically connected to ones of the conductive traces. An intermetallic heat spreader 130 is fixed to a backside of the semiconductor die 124 and a plurality of contact balls 128 are disposed on the second surface of the substrate. The contact balls 128 are in the form of a ball grid array and ones of the contact balls 128 of the ball grid array are electrically connected with ones of the conductive traces of the substrate 122.

[0020] The flip-chip BGA package 120 will now be described in more detail with reference to the sectional view of the flip-chip BGA package 120 of Figure 2. The flip-chip BGA package 120 includes the substrate 122 of a BT resin/glass epoxy printed circuit board 140 with conductive traces for signal transfer. The conductive traces are typically copper and connect the interconnect pads on the first side of the substrate 122 and contact pads on the second side of the substrate 122. Interconnect pads and contact pads are connected by the copper conductive traces of the substrate 122 that extend therebetween. The interconnect pads connect with the solder ball electrical connectors 126 of the semiconductor die 124 and the contact pads connect with the contact balls 128 of the ball grid array. A solder mask is deposited on the upper and lower surface of the substrate 122, with the interconnect pads and the contact pads of the conductive traces exposed.

[0021] The semiconductor die 124 is flip-chip mounted to the upper surface of the substrate 122. The semiconductor die 124 is mounted to the substrate 122 by solder ball connection of pads of the semiconductor die 124 with the interconnect pads of the substrate 122. The solder balls 126 are placed on the substrate 122 using known pick and place and reflow techniques. Preferably the solder balls 126 are made of solder with a reflow temperature greater than the reflow temperature of eutectic solder. It will be appreciated that the pads of the semiconductor die 124 align with the interconnect pads of the substrate 122 and the solder balls 126 electrically connect the semiconductor die 124 with the interconnect pads.

[0022] The area under the semiconductor die 124 is filled with a thermosetting plastic compound, referred to generally as an underfill material 132. The underfill material 132 surrounds the solder balls 126 that connect the semiconductor die 124 and the interconnect pads of the substrate 122. The underfill material 132 serves to absorb some of the thermally induced stresses.

[0023] The intermetallic heat spreader 130 is in the form of a plate of intermetallic compound and is fixed to the backside of the semiconductor die 124 using a thermally

conductive adhesive or thermally conductive epoxy.

[0024] Intermetallic compounds, also referred to as intermetallics are chemical compounds based on definite atomic formulas, each with a fixed or narrow range of chemical composition. The intermetallic compounds are stoichiometric combinations of metallic ions that form bonded matrices of compounds, the properties of which vary significantly. In the present embodiment, the intermetallic heat spreader 130 is made of an intermetallic compound that has a coefficient of thermal expansion (CTE) in the range of about 18 ppm/°C to about 26 ppm/°C and preferably has a CTE of about 22 ppm/°C. A high elastic modulus is also desirable for restraining the semiconductor die 124 during thermal cycling when the package 120 is in use. A particularly suitable intermetallic compound is copper aluminide ($CuAl_3$), which has a CTE of about 22 ppm/°C and an elastic modulus higher than that of the semiconductor die 124.

[0025] Solder balls 128, commonly referred to as solder bumps, are placed on the contact pads on the second side of the substrate 122 and reflowed using known pick and place and reflow techniques. The solder balls 128 are a eutectic solder having a lower reflow temperature than the solder balls 126 between the semiconductor die 124 and the substrate 122. This permits reflow of the solder balls 128 without significant reflow or movement of the solder balls 126 between the semiconductor die 124 and the substrate 122. Clearly the solder balls 128 are electrically connected to the pads of the semiconductor die 124 via the solder balls 126, and the conductive traces and the contact pads of the substrate 122.

[0026] Reference is now made to Figure 3 to describe a second embodiment of the flip-chip BGA package of the present invention. In this embodiment, the intermetallic heat spreader 130 includes a first flat portion 134 that is fixed to the backside of the semiconductor die 124 and four sidewalls 136 that extend downwardly from the first flat portion, to the substrate 122. Only two of the four sidewalls 136 are shown in the sectional view of Figure 3. The sidewalls 136 are fixed to the substrate using a thermally conductive adhesive or epoxy, thereby providing additional support and stiffness for the BGA package 120. The remainder of the elements of the present embodiment are similar to those of the first-described embodiment and need not be further described herein.

[0027] Reference is now made to Figure 4 to describe a third embodiment of the flip-chip BGA package of the present invention. In this embodiment, the intermetallic heat spreader 130 is a flat plate that is fixed to the backside of the semiconductor die 124. Four sidewalls 136 are fixed between the intermetallic heat spreader 130 and the substrate 122, at the periphery of the

intermetallic heat spreader 130. The sidewalls 136 are fixed to the heat spreader 130 prior to fixing the heat spreader 130 to the semiconductor die 124 and are fixed to the substrate when the heat spreader 130 is fixed to the semiconductor die 124. The sidewalls 136 are fixed to the heat spreader 130 using a thermally conductive epoxy or adhesive, and similarly, the opposing end of the sidewalls 136 are fixed to the substrate using a thermally conductive epoxy or adhesive. The sidewalls 136 can be made of any suitable material including, intermetallic compound, ceramic or metal such as copper, nickel or iron based metals. The sidewalls 136 provide additional support and stiffness for the BGA package 120. The remainder of the elements of the present embodiment are similar to those of the first-described embodiment and need not be further described herein.

[0028] The present invention has been described by way of example. Modifications and variations to the embodiments described herein may occur to those skilled in the art. For example, the intermetallic heat spreader is not limited to $CuAl_3$ and other suitable intermetallic compounds can be used, including NiAl. Still other suitable intermetallic compounds can be used. A list of several intermetallic compounds is included in the attached Appendix A and any suitable intermetallic compound having the desired material properties can be chosen from this list. Still other suitable intermetallic compounds may be possible. Also, the second and third-described embodiments are described as having four sidewalls, however, other numbers of sidewalls are possible. For example, two sidewalls can be used. Still other modifications and variation are possible, all of which are within the sphere and scope of the present invention.